AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method of routing IP packets ~~between a plurality of circuit cards~~ within a node of a network, comprising:

receiving a packet at ~~an~~ a first interface circuit ~~interfaces~~ within the node, the packet being an IP packet and including a label stack, the label stack including an external routing label for use in forwarding between nodes along a label-switched path;

pushing, at the first interface ~~interfaces~~, an internal routing label on to the label stack of the packet to create a modified packet, the internal routing label specifying a packet type; the internal routing label further specifying an address for a second ~~one of the plurality of circuit cards~~ interface circuit within the node if the packet type is of a first type, and specifying the address of the first interface circuit if the ~~and a~~ packet type is of a second type, the second type being a type indicative of a control packet;

routing with a switch within the node the modified packet to the second ~~one of the plurality of circuit cards~~ interface circuit specified in the internal routing label in response to the packet type being indicative of a first type and to a control circuit associated with the second type if the packet is of the second type.

2. (Currently amended) The method, as set forth in claim 1, wherein routing the modified packet to the second ~~one of the plurality of circuit cards~~ interface circuit comprises routing each modified packet by at least a shelf and slot numbers for a circuit card comprising the second interface circuit, the shelf and slot numbers being included in the internal routing label.

3. (Currently amended) The method, as set forth in claim 1, wherein routing the modified packet to the second interface circuit ~~one of the plurality of circuit cards~~ comprises routing each modified packet based on a shelf identifier, a slot identifier, a link identifier, and a

channel identifier for a circuit card comprising the second interface circuit, the shelf identifier, slot identifier, link identifier and channel identifier being included in the internal routing label.

4. (Currently amended) The method, as set forth in claim 32, wherein sending the reply packet to ~~one of the plurality of circuit cards~~ the first interface circuit comprises routing the reply packet ~~to the one of the plurality of circuit cards~~ based on an address contained in a second internal routing label included with the reply packet, the address in the second internal routing packet including the shelf and slot numbers included in the address of in the internal routing label of the modified packet.

5. (Currently amended) The method, as set forth in claim 32, wherein sending the reply packet to the ~~one of a plurality of circuit cards~~ first interface circuit comprises routing the reply packet based on a shelf identifier, a slot identifier, a link identifier, and a channel identifier included in the internal routing label for the modified packet ~~transporting the reply packet~~.

6. (Currently amended) The method, as set forth in claim 1, wherein routing the modified packet to the second interface circuit ~~to the one of a plurality of circuit cards~~ comprises:

receiving, from the interface, the packet at a switch; and

switching the modified packet to the one of the ~~plurality of circuit cards coupled~~ to a predetermined port of the switch as specified by shelf and slot numbers ~~of~~ comprising the address ~~destination~~ included in the internal routing label.

7. (Currently amended) The method, as set forth in claim 1, wherein routing the modified packet ~~to the one of a plurality of circuit cards~~ to the second interface circuit comprises:

receiving~~, from the interface,~~ the modified packet at a switch; and

routing the modified packet ~~to the one of a plurality of circuit cards coupled~~ to a predetermined port of the switch as specified by a shelf identifier, a slot identifier, a link identifier, and a channel identifier comprising the address included in the internal routing label.

8. (Currently amended) The method, as set forth in claim 32, wherein routing the modified packet to the control circuit ~~a processor~~ and sending the reply packet comprises:

receiving~~, from the interface,~~ the modified packet at a switch;

switching the modified packet to a predetermined port of the switch coupled to the processor; and

switching the reply packet ~~to the one of the plurality of circuit cards coupled~~ to a second predetermined port of the switch specified by shelf and slot numbers included in the internal routing label.

9. (Currently amended) The method, as set forth in claim 32, wherein routing ~~each~~ the modified packet to the [~~a~~] processor and sending the reply packet to one of the plurality of circuit cards comprises:

receiving~~, from the interface,~~ the ~~each~~ modified packet at [~~a~~] the switch;

switching the modified packet to a predetermined port of the switch coupled to the processor; and

switching the reply packet to the ~~one of the plurality of the circuit cards coupled to a second predetermined port of the switch specified by a~~ first interface card, the reply packet containing a second internal routing label specifying the shelf identifier, [~~a~~] the slot identifier, [~~a~~] the link identifier, and [~~a~~] the channel identifier included in the internal routing label for ~~transporting the reply~~ the modified packet.

10 -11. (Cancelled)

12. (Previously presented) The method, as set forth in claim 1, further comprising popping the internal routing label from the label stack on the modified packet after receiving the modified packet at the one of the plurality of circuit cards.

13. (Currently amended) The method, as set forth in claim 32, further comprising popping the internal routing label from the label ~~information table~~ stack after receiving the modified packet at the ~~processor~~ control circuit within the node.

14-24. (Cancelled)

25. (Previously presented) The method, as set forth in claim 1, further comprising popping the internal routing label from the label stack after receiving the packet at a processor within the node.

26 – 27. (Cancelled)

28. (Currently amended) The method, as set forth in claim 1, wherein routing the modified packet to the ~~one of the plurality of circuit cards~~ second interface circuit comprises:

receiving, from the first interface circuit, the modified packet at a switch; and

switching the modified packet to a predetermined port of the switch coupled to the ~~one of the plurality of circuit cards~~ the second interface circuit specified in the internal routing label.

29. (Currently amended) The method, as set forth in claim 1, wherein routing the modified packet to the one of the plurality of circuit cards comprises:

receiving, from the first interface circuit , the packet at a switch; and

switching the modified packet to the one of the plurality of circuit cards coupled to a predetermined port of the switch as specified by at least a shelf identifier and slot identifier, included in the internal routing label ~~for transporting the packet~~.

30. (Cancelled)

31. (Cancelled)

32. (Currently amended) The method of claim 1, further comprising ~~routing the modified packet to a processor within the node and~~ sending a reply packet to the ~~one of the plurality of circuit cards~~ first interface circuit specified in the internal routing label in response to the packet type being indicative of a control packet.

33. (Currently amended) An apparatus at a node of a network, comprising:

a plurality of addressable circuits ~~cards~~ and a switching fabric, the plurality of addressable circuits comprising at first interface circuit and a second interface circuit;

the first circuit comprising means for receiving a packet, the packet being an IP packet and including a label stack, the label stack including an external routing label for use in forwarding between nodes along a label-switched path;

the first circuit further comprising means for pushing an internal routing label to the label stack of the packet to create a modified packet, the internal routing label including a packet type identifier and an address of one of the plurality of addressable circuits, the address specifying the second interface circuit, from which the modified packet will by transmitted by the apparatus to another node, if the packet type identifier indicates a data type, and specifying the first interface circuit the packet type identifier is of a control type;

the switching fabric including means for routing the modified packet through the switching fabric to one of the plurality of circuits ~~circuit cards~~ based on the internal routing label attached to the modified packet, the means for routing routing the modified packet based on the address in the internal routing label if the packet type identifier indicates a data type; ~~and~~

the second interface circuit comprising means for removing the internal routing label prior to transmission of the packet from the apparatus.

34. (Currently amended) The apparatus of claim 33, ~~further comprising~~: wherein the control circuit is comprised of a processor, the processor including means for sending a reply packet, in response to receiving a modified control packet, to one of the plurality of circuit cards identified in the internal routing label.

35. (Cancelled)

36. (Cancelled)

37. (Currently amended) The apparatus of claim 33 [[35]], wherein the means for routing includes means for routing the modified packet to ~~the processor~~ a control circuit based on the packet type if the packet type identifier indicates a control packet type.

38. (Currently amended) The apparatus of claim 33, wherein the internal routing label includes at least one field for identifying the location of one of the plurality of the circuits ~~circuit cards~~ within the node.

39. (Currently amended) The apparatus of claim 38, wherein the at least one field for identifying the location of one of the plurality of circuits ~~circuit cards~~ within the node includes identifiers for a shelf and a slot of a card for the one of the plurality of circuits ~~circuit cards~~.

40. (Currently amended) The apparatus of claim 33, further comprising memory for storing a routing table, the routing table including fields for the external label and the internal routing label.